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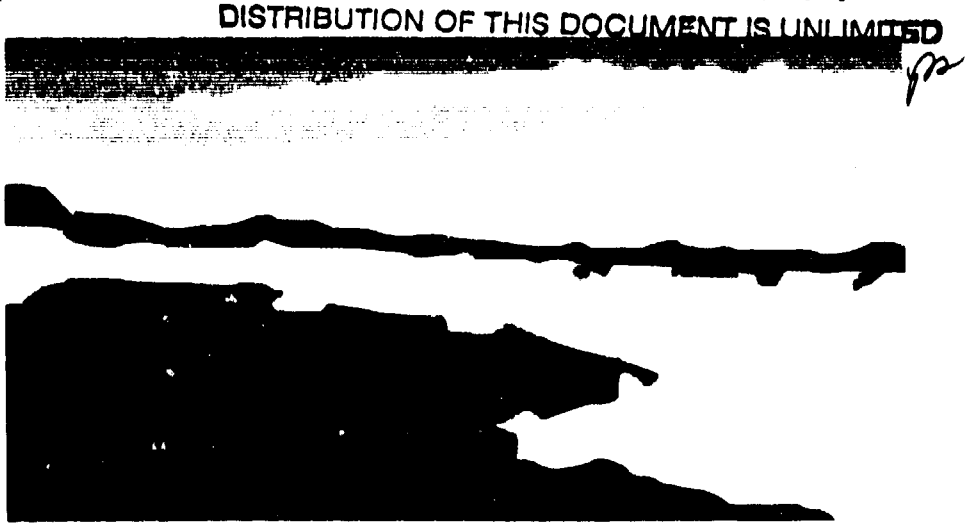

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Recent Developments in Multiplicity Counting Hardware at Los Alamos*

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Abstract

This paper describes a prototype, 256-channel neutron-multiplicity-counting circuit. It is being used with a 4-MHz shift-register-based neutron coincidence circuit. We developed both circuits. They mount in a double-wide nuclear instrument module.

I. INTRODUCTION

Neutron coincidence counting has played an important role in determining the mass of fissile material in safeguards and nuclear industry samples. The principle is simple; the mass of material is proportional to the *spontaneous* fission rate. During the fission process, multiple neutrons are emitted within a very short time frame, that is, in coincidence. The number of neutrons emitted in coincidence determines the multiplicity of the event. The challenge is to determine the spontaneous fission rate from measured neutron multiplicity distributions.

Both spontaneous fissions and induced fissions contribute to the coincidence rate of neutrons emitted from a sample. Induced fissions are caused by neutrons from outside the nucleus. These neutrons could have been neutrons given off by a previous spontaneous or induced fission or by (α,n) reactions if the sample contains low-Z-element impurities (for example, oxygen or fluorine). The induced-fission neutrons are termed multiplication neutrons. (Note: Multiplication is different from multiplicity.) Three variables exist in the generation of coincidence neutrons: sample mass, (α,n) interactions, and multiplication.

A classical limitation of coincidence counting assay has been that only two independent quantities are measured: total neutron counts and real coincidences. In general, corrections must be applied to measured results to get accurate assays. Exceptions are the assay of pure metals in which there are no (α,n) interactions or of pure oxides for which low-Z material is well characterized. In both cases, well-established multiplication corrections can be applied. Accurate corrections can also be made if the sources are well characterized with regard to impurities in the sample that give rise to (α,n) reactions. In reality the characterization of samples measured for safeguards is often not well known. By determining the distribution of coincidence multiplicities of neutrons emitted from a sample, one can extract three independent variables from a multiplicity measurement.[1]

The multiplicity distribution detected by coincidence counters is often dominated by accidental coincidences, which are a function of neutron count rate and coincidence gate width. Analytical methods have been developed to remove the accidental coincidences from the measured distributions.[1,2] A key point is that the analysis to remove the accidental coincidences has been developed for a specific configuration of the hardware.

Our initial work using multiplicity to solve accuracy problems in nuclear safeguards made use of an 8-channel multiplicity electronics package.[1,3] Later a 32-channel version was developed and used for multiplicity detector design and assay investigations.[4] But this too had insufficient multiplicity capacity to allow study of the desired range of sources without drastically reducing normal detector die-away times or efficiencies thereby increasing statistical counting errors. These unacceptable solutions drove the development of our current 256-channel multiplicity electronics design.

In this paper we describe how our multiplicity circuitry operates in conjunction with existing coincidence electronics and report on initial circuit performance tests.

II. THE SHIFT-REGISTER COINCIDENCE COUNTER

The operation of our shift-register coincidence circuitry has been described in detail.[5,6] Briefly, coincidence neutrons are emitted from a sample into a detector. The neutrons bounce about in the polyethylene of the detector, lose energy, and are absorbed by ^{3}He tubes, cadmium, or polyethylene in the detector. The charge from an interaction in the tube is changed by a preamplifier into a digital pulse of approximately 35 to 50-ns duration. Neutrons in a detector have a characteristic die-away time, which is the time a population of neutrons in a detector will have decayed to e^{-1} of the original population. The probability of neutrons surviving in the detector for a length of time equal to n die-away times is e^{-n}. For a typical detector the die-away time would be approximately 40 μs. The probability of a neutron surviving 1 ms is 1.4×10^{-11}. The shift register typically counts the number of neutrons that occur in a 64-μs window from the time a neutron is detected. This number represents neutrons that were actually emitted in

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coincidence with the reference neutron (a real coincidence) as well as other neutrons (accidental coincidences) that happened to be in the detector at that time—perhaps from another fission, an (α,n) interaction in the source, or perhaps it was a background event. The measured number includes real plus accidental coincidences (R+A). If one measures the number of neutrons in a window between 1.000 ms and 1.064 ms, one will measure a number statistically equal to the accidental coincidences (A) in the first window. Hence by subtracting the A counts from the R+A counts one statistically determines the net real coincidences.

A block diagram of a circuit that makes this measurement is shown in Fig. 1. It is a diagram of the SR-4 circuitry developed by Los Alamos, in part, to test the feasibility of a multiplicity measurement's capability to increase the accuracy of fissile material assays.

Signals from a detector preamplifier/discriminator are synchronized to the synchronous system clock just after input. The synchronizer is like a storage hopper where signals are received asynchronously. The signals are let out of the hopper, at a rate of one signal per compartment, on a conveyor belt with discrete compartments along its length. Signals coming in faster than the conveyor rate are temporarily stored in the hopper and released at the synchronous rate. If the signals enter slower than the conveyor rate, they immediately fall onto the conveyor. The conveyor is shown by the double lines connecting the gate shift register (GSR), the predelay shift register (PDSR), and the long-delay shift register (LDSR). The shift registers can be thought of as long tunnels through which the conveyor travels. Once the conveyor enters the tunnel, information on the part of the conveyor inside the tunnel is hidden from the outside world. The tunnels are of different (and programmable) lengths.

In our example, signals that enter the GSR cause a counter to be incremented; those that exit cause the same counter to be decremented. Hence the up/down counter knows the number of signals inside the tunnel at any specific moment in time. Immediately after the signal exits the GSR tunnel it enters the PDSR tunnel. When the signal exits this tunnel, it causes the contents of the GSR to be counted as the number of coincidences (R+A) with that signal. The signal then

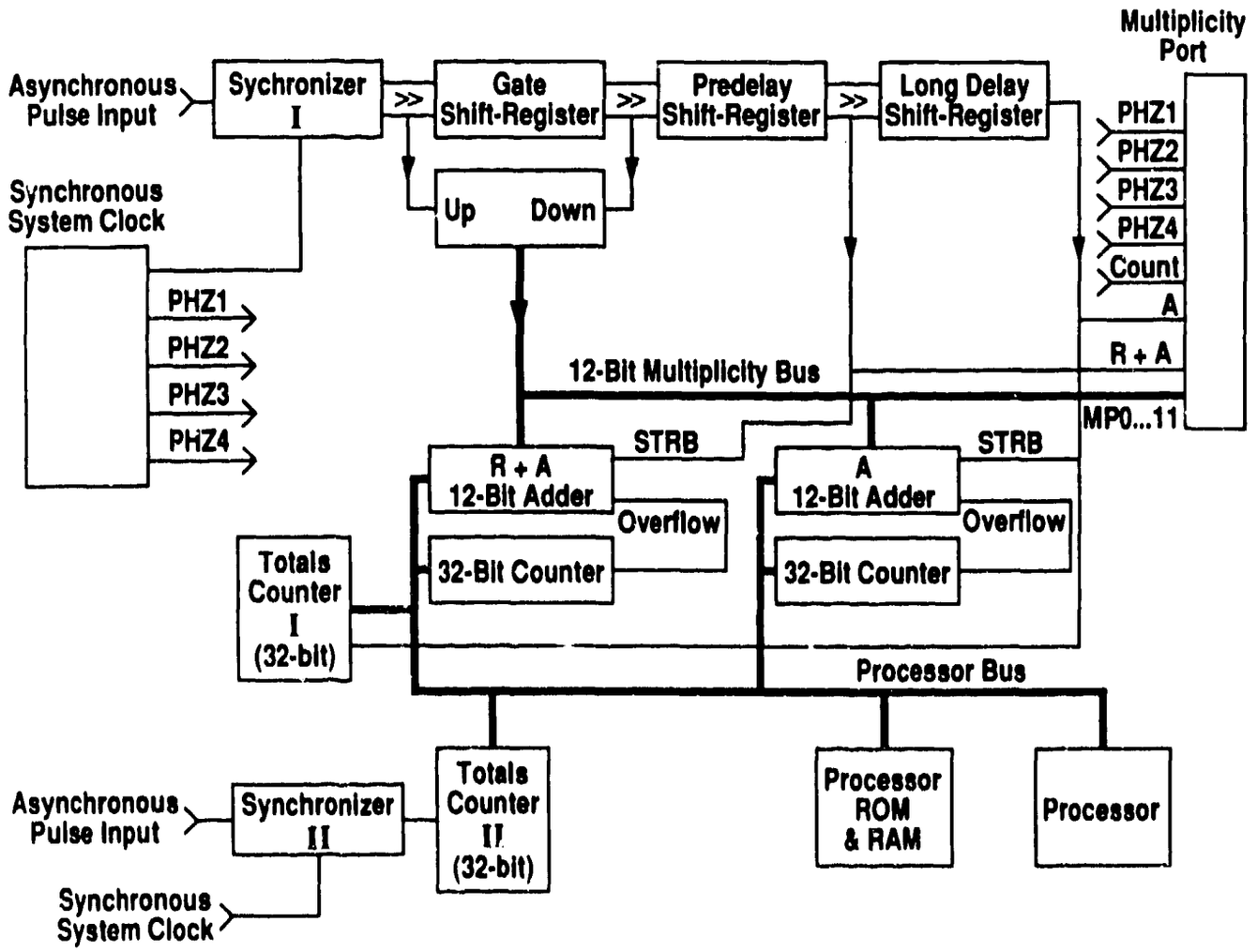

Fig. 1. Block diagram of shift-register coincidence counter circuit.

immediately enters the LDSR tunnel. When the signal exits this tunnel, it causes the contents of the GSR to be counted as the number of accidental coincidences. The signal is then no longer of interest and is forgotten.

In physical terms, the GSR is the time window in which neutrons exist that are considered to be in coincidence with the neutron exiting the PDSR. After a neutron has exited the LDSR, any neutrons that were emitted in coincidence with the exiting neutron will have died away, and hence the number of neutrons in the GSR is a statistical measure of the number of "accidental" coincidences included in the number of coincidences recorded after the neutron exited the PDSR. The statistical net number of "real" coincidences is the difference between the R+A sum and the A sum.

The total number of coincidences for a data acquisition are summed in a two-step process. The contents of the GSR are summed in a 12-bit adder. The overflows of this adder are counted in a 32-bit adder. This results in a 44-bit *real-time* scaler for each of the R+A and A channels.

The multiplicity of an event is measured by the number of neutrons in the GSR when a neutron exits the PDSR (R+A multiplicity) or the LDSR (A multiplicity).

The totals sum is the sum of all neutrons that pass through the conveyor. The totals counter is incremented each time a neutron exits the LDSR.

Note: The PDSR is required because effective system deadtime prevents additional signals within a short period of a sensed signal from being detected. These signals are effectively removed from the R+A counter. Because no similar process occurs for the A counter, a PDSR is inserted that affects both A and R+A and is set for a delay that is longer than effective system deadtime.

III. MULTIPLICITY PROCESSING

Our goal in this project was to provide hardware for investigating the feasibility and limitations of multiplicity counting with standard counters and hardware. Our goal was to have real-time processing of multiplicity from the SR-4 shift register implemented simply, in minimal size, and relatively low power. (Real-time processing means that we can, on the average, process multiplicity as fast as the shift-register circuit can operate.) The circuit was to fit in a nuclear instrumentation module (NIM) that houses the SR-4. A multiplicity capacity of 256 channels was needed for the assay of significant quantities of nuclear materials.

The engineering problem was to take the multiplicity information—the contents of the GSR—and record the multiplicity distribution information at an average rate of 2.3×10^6 events/s. This number was inferred from empirically determined performance of a shift register operating at 2 MHz.[7]

Our approach is explained with the aid of Figs. 1 and 2. The multiplicity port shown in Fig. 1 consists of the 12-bit output of the GSR-contents up/down counter, the R+A and A strobes for the PDSR and the LDSR, the four-phase clock signals, and a count-active control signal.

Our multiplicity counter is really two sets of counters (Fig. 2): one set for R+A events and the other for A events. The counter sets are identical and each set has two stages. The first stage is a 256-channel counter with each channel being 8 bits deep. Overflows from any of these channels cause the channel number to be saved and a flag to be set. The flag indicates the microprocessor needs to read the overflowing channel number and increment a software counter associated with the hardware counter that has overflowed. The 8-bit hardware counter reduces the increment duty cycle required for the microprocessor, that is, the microprocessor needs to respond (on the average) to only every 256th event from the SR-4. The microprocessor provides a means of reducing hardware required for the multiplicity counter and provides for readout of the multiplicity data.

The following description of circuit operation is for the R+A set of counters. The A set operates identically. The clock of the SR-4 operates at 4 MHz. The multiplicity counter requires the SR-4 clock cycle to be divided into 4 phases. (The original SR-4 required only two phases.)

During each 4-MHz clock cycle of the SR-4, the multiplicity information and the status of the R+A and A data strobes are presented to the multiplicity port of the SR-4. These data are latched on one of the four phases of the SR-4 clock data into the multiplicity board. Hence the multiplicity processing of the information through the first 8-bit counter must be completed in an SR-4 clock cycle, 250 ns.

During an acquisition, the SR-4's multiplicity output is applied to the address lines of a RAM in the multiplicity circuitry. The contents of the location addressed is output on the RAM's data lines. The value output is incremented by one in an adder circuit, and the sum is latched. *Only* if there is an active R+A data strobe from the SR-4 is the sum written back into the RAM. When the counter overflows, the address being presented to the RAM is latched into a FIFO, and a flag is set to signal the microprocessor. At the end of the 250-ns period this process is repeated.

The microprocessor continuously and asynchronously polls the status of the overflow flag. When an active flag is encountered, the microprocessor reads the FIFO to determine the overflowing channel and then increments the appropriate software counter. The program can comfortably keep pace with the interrupts. The worst case exists when both R and R+A strobes are active on the same SR-4 pulse. The time for the microprocessor to complete its cycle is 94 μs, which is less than 115 μs ($256 \times 2.3 \times 10^{-16}$), the average time in which it must respond.

When the SR-4 signals the end of an acquisition, the hardware grants the microprocessor read access to the 8-bit counters. The microprocessor concatenates the corresponding software and hardware counters and transfers the resulting data to the computer controlling the SR-4 on request from the

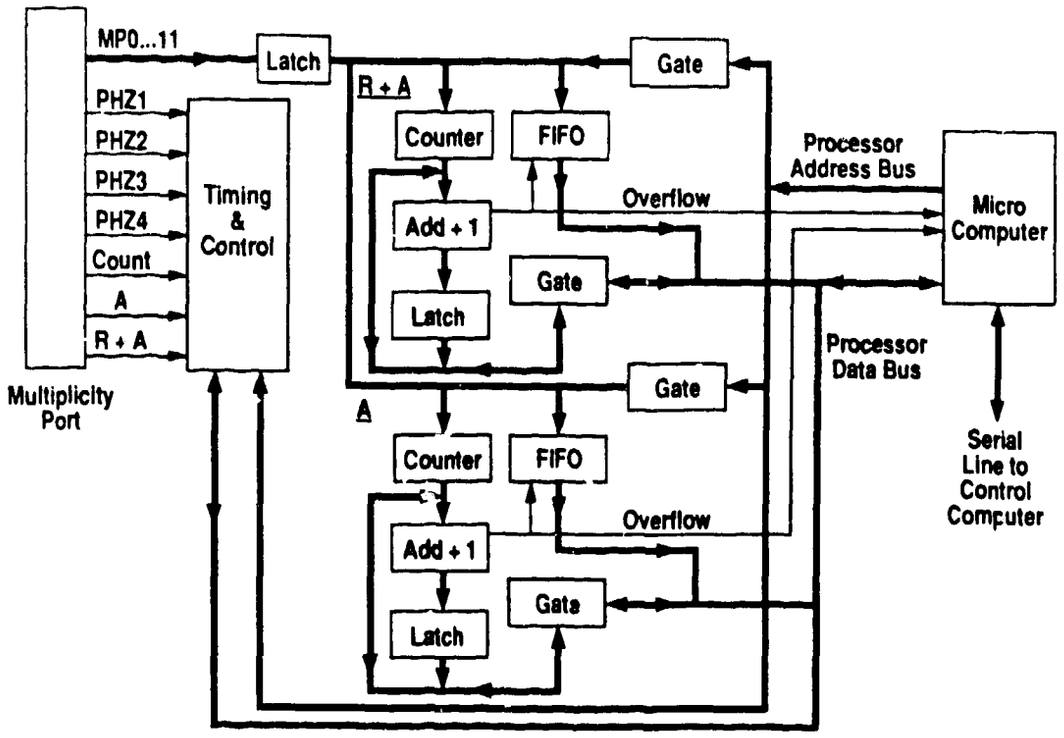

Fig. 2. Block diagram of multiplicity-counter circuit.

computer. Dynamics of the SR-4 require that the up/down counter be 12 bits wide. The multiplicity requirements require only 8 bits. Hence the high-order four bits are logically ORed together. If this OR is true, all of the eight multiplicity bits are set to 1. The result is a true 0-254 multiplicity counter and channel 255 counts all multiplicities of 255 and greater.

IV. RESULTS

We have produced a double-wide NIM module version of the hardware (Fig. 3). This implementation requires separate serial interfaces for the SR-4 and multiplicity circuits. The SR-4 board is mounted in Fig. 3, and the multiplicity board is dismounted. For performance evaluation, a program was written to control and receive data from the hardware. Two very simple and powerful diagnostics can be applied to this circuitry. The SR-4 totals should equal the sum of the accidental multiplicity events. In addition, the R+A and A coincidences counted by the SR-4 should equal sums of the R+A and A multiplicities multiplied by the multiplicity (channel)/ number.

The coincidence data from an AmLi source is shown in Table I(a). Table I(b) is the multiplicity data measured at the same time. This data had no multiplicities >65 or <5. Table I(a) shows the SR-4 setup parameters and results. In Table I(b), the left-hand column is the multiplicity number.

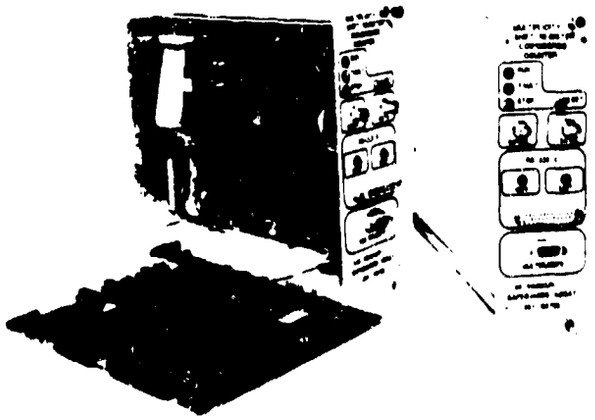

Fig. 3. Package for shift-register and multiplicity-counter circuits.

The middle column is the number of times that multiplicity occurred in R+A coincidences. The right-hand column is the same number for the A coincidences. The numbers at the bottom of the two right-hand columns represent the sums of numbers in the column. Notice that the sum of the A-column multiplicities equals the totals measured by the SR-4. The sum of the R+A column does not always equal the totals because the timing interval used for the R+A's, while equal in time to that of the A's, is shifted

TABLE I(a). Shift-Register Output

Set Count Time (s)	1 000
Gate Width (μs)	60
Predelay (μs)	1.5
Actual Count Time (s)	1 000
Totals	480 382 540
Reals + Accidentals (R+A)	13 846 354 321
Accidentals (A)	13 846 092 846
Reals ([R+A] - [A])	261 475

from that of the A's by approximately 16 ms. The weighted sums (products of the multiplicities and the contents of the column entries) are also listed at the bottom of the columns. Note these values equal the values in the R+A and A registers of the SR-4.

V. SUMMARY

We have found that occasionally the sum of the A events differs from the totals. We believe the cause is a problem in synchronization of the "COUNT" signal that enables multiplicity counting. This hypothesis will be tested.

The prototype multiplicity shift register is now being tested in the Plutonium Facility at Los Alamos. Our physicists are satisfied with its operation and multiplicity capacity. From an engineering standpoint, the system is working as desired (with the exception noted above).

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TABLE I(b). Multiplicity-Counter Results

Muluplicity	R+A	A
5	14	25
6	74	62
7	247	282
8	912	924
9	3158	3168
10	9769	9628
11	27224	27094
12	68314	68369
13	158472	157803
14	340023	340446
15	682411	679763
16	1277458	1278202
17	2244013	2244843
18	3715383	3714077
19	5813667	5811781
20	8619056	8617374
21	12135375	12139587
22	16275181	16273563
23	20810255	20806538
24	25401957	25410154
25	29713647	29709942
26	33289622	33294907
27	35814993	35821643
28	37051562	37065829
29	36926369	36931235
30	35453201	35451536
31	32842996	32849678
32	29397415	29403235
33	25436845	25436991
34	21310234	21301206
35	17294146	17280965
36	13597370	13595113
37	10373323	10369253
38	7680676	7673479
39	5520573	5519024
40	3862633	3861741
41	2629001	2628824
42	1744117	1743175
43	1125831	1125461
44	704943	706362
45	431990	432768
46	259247	258814
47	150602	150295
48	86373	85609
49	48052	48189
50	26016	25736
51	13712	13702
52	7220	7092
53	3518	3569
54	2011	1873
55	901	903
56	465	404
57	169	200
58	71	74
59	33	17
60	6	3
61	1	1
62	0	3
63	5	5
64	1	0
65	0	1
Sum	480382853	480382540
Weighted Sum	13846354321	13846092846